REMARKS

This is a full and timely response to the outstanding final Office Action mailed March 7, 2005 (Paper No. 20050303). Upon entry of this response, claims 70-74 and 80-83 are pending in the application. In this response, claims 75-79 and 84-102 are cancelled. Applicant respectfully requests that the amendments being filed herewith be entered and request that there be reconsideration of all pending claims.

1. Response to Restriction Requirement

The Office Action alleges that claims 88-102, added in the last response, are directed to an invention that is independent or distinct from the invention originally claimed. The Examiner has withdrawn claims 88-102 from consideration. Claims 88-102 are cancelled in this response. Applicant expressly reserves the right to present withdrawn claims 88-102, or variants thereof, in continuing applications to be filed subsequent to the present application.

The Office Action further requires Applicant to elect to prosecute one of two groups of the remaining claims. In response to this restriction requirement, Applicant elects to prosecute the claims of Group I, corresponding to claims 70-74 and 80-83. Claims 75-79 and 84-87 are cancelled. Applicant expressly reserves the right to present withdrawn claims 75-79 and 84-87, or variants thereof, in continuing applications to be filed subsequent to the present application.

2. Rejection of Claim 70 under 35 U.S.C. §102

Claim 70 has been rejected under §102(b) as allegedly anticipated by *Byers et al.* (U.S. 5,524,218). Applicant respectfully traverses this rejection. A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. *See, e.g., W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir.

1983). Applicant respectfully submits that *Byers et al.* does not disclose, teach, or suggest the feature of "a digital signal processor" as recited in claim 70.

The Office Action asserts that FIG. 4B of *Byers et al.* includes microprocessors (μSBCs) 164 and 166. The Office Action further asserts that FIG. 4B includes an LPFC 178 that processes digital data under the control of the μSBC microprocessor. The Office Action then concludes that "[t]he device taught Figure 4B is a device for processing digital data subject to executable instructions; hence is a digital signal processor." (Office Action, pages 5-6.)

Applicant respectfully disagrees with the reasoning of the Office Action. namely, that μSBC 164 in combination with LPFC 178 is a "digital signal processor." Applicant first points out that μSBC 164 in *Byers et al.* is a reduced instruction set (RISC) microprocessor (Col. 7, lines 48-60), and that LPFC 178 is a gate array (Col. 8, lines 15-20). Applicant will also assume, *arguendo*, that the gate array 178 "processes digital data." Even so, Applicant disagrees with the reasoning and conclusion of the Office Action that a RISC microprocessor in combination with gate array is a "digital signal processor" because it "processes digital data subject to executable instructions."

Applicant has enclosed a 37 C.F.R. §1.132 affidavit (see Exhibit A) as evidence that one skilled in the art would understand the term "digital signal processor" to mean a processor with a specific type of architecture. As explained in the affidavit, a "digital signal processor" is characterized by certain architectural features.

Byers et al. describes the following features of μSBC 174: it is a RISC microprocessor; it supports an instruction set of seven basic instructions; and it is not micro-programmed. (Col. 7, lines 45-65.) These features are not equivalent to the features of a digital signal processor as

explained in the affidavit of Exhibit A. Thus, there is no suggestion or teaching in *Byers et al.* that μSBC 174 is a "digital signal processor" as that term is understood by one skilled in the art.

For at least the reason that *Byers et al.* fails to disclose, teach or suggest "a digital signal processor," Applicant respectfully submits that *Byers et al.* does not anticipate claim 70. Therefore, Applicant requests that the rejection of claim 70 be withdrawn.

3. Rejection of Claims 71-74 and 80-83 under 35 U.S.C. §103

Claims 71-74 and 80-83 have been rejected under §103(a) as allegedly obvious over *Byers et al.* (U.S. 5,524,218) in view of *Aoyagi et al.* (U.S 4,613,975). Applicant respectfully traverses this rejection. Since claim 70 is allowable for at least the reasons discussed above, Applicant respectfully submits that claims 71-74 and 80-83 are allowable for at least the reason that each depends from an allowable claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir. 1988). Therefore, Applicant respectfully requests that the rejection of claims 71-74 and 80-83 be withdrawn.

CONCLUSION

Applicant respectfully requests that all outstanding objections and rejections be withdrawn and that this application and presently pending claims 70-74 and 80-83 be allowed to issue. If the Examiner has any questions or comments regarding Applicant's response, the Examiner is encouraged to telephone Applicant's undersigned counsel.

Respectfully submitted,

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EXHIBIT "A"

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Joseph Quinn Chapman

Serial No.: 09/716,787

Filed: November 20, 2000

Group Art Unit: 2133

Examiner: Torres, Joseph D.

Docket No. 061606-1241

For: Apparatus and Method to Allow a Frame Check Sequence to Determine the Updating of Adaptive Receiver Parameters of a High Speed Communication Device

AFFIDAVIT OF KENNETH D. KO

UNDER 37 C.F.R. 1.132

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

I, Kenneth D. Ko, declare as follows:

Education and Experience

1. I am an employee of the assignee of the 09/716,787 application.

2. I graduated from the Georgia Institute of Technology with a B.S.E.E. (Bachelor of Science in Electrical Engineering) degree in 1980, and from the University of South Florida with an M.S. degree in Electrical Engineering (with emphasis in Digital Signal Processing and Communications) in 1987.

3. I am an inventor or co-inventor on 29 U.S. patents.

4. I have participated in international, regional, and national standards committees, including the ITU (International Telecommunications Union), ETSI (European

Telecommunications Standards Institute), TIA (Telecommunications Industry Association), ATIS (Alliance for Telecommunications Industry Solutions), DSL Task Group (United Kingdom), TTC (Telecommunication Technology Committee, Japan), and DSL Forum since 1994.

5. I have worked for 17 years on systems which use digital signal processors, including digital subscriber loop modems, voice frequency modems for both dial and leased lines, and speech encoder/decoders. I have worked with both hardware and embedded software for these systems. I began as a hardware developer, then transitioned to software/firmware development, then to architect and lead developer of a hardware and firmware group. I have been actively working on design of DSP-based sub-systems since 1988, and have developed numerous designs using digital signal processors, FPGA's, ASICs, and embedded firmware for digital signal processors. In the normal course of this work, I have become very familiar with the architecture and the functional characteristics of various digital signal processors, including: TMS320C5x, TMS320C6x, and other DSP families from Texas Instruments; AT&T DSP16A; and proprietary DSP designs developed within Paradyne and Rockwell Semiconductor Systems (now Conexant), including DSPs to which I contributed design elements.

6. Through my education and work in the electronics industry, I have gained extensive experience with digital signal processing, digital signal processors, and firmware executing on digital signal processors.

The Byers et al. Reference (U.S. 5,524,218, herein Byers)

7. The Patent Examiner who is responsible for examining the above-noted patent application had the following comments to make in the "Response to Arguments" section of the Office Action mailed March 7, 2005:

> [The Examiner] asserts that Figure 4B in Byers teaches that USBCs are microprocessors as the Applicant acknowledges on page 15 of the applicant's current response for executing instructions from an instruction set. LPFC 178 in Figure 4B of Byers processes digital data under the control of USBCs 164 and 166 in Figure 4B. ***The device taught in Figure 4B is a device for processing digital data subject to executable instructions; hence is a digital signal processor.*** (Emphasis added)
> (Office Action, p. 6.)

8. *Byers* discloses, in col. 7, lines 48-60, that the μSBC (Microsequencer Bus Controller) referred to by the Examiner is a microprocessor with a reduced-instruction set architecture:

> The architecture of the DM 48 as an instance of a Microsequencer Bus Controller System shows that there are two Microsequencer Bus Controllers (uSBCs) 94, 96 connected to a Control Store (CS) 98 via Lines 100, 102. The uSBC 0 94 and uSBC 196 are Reduced Instruction Set (RISC) microprocessors that control various special purpose gate arrays called Stations connected to the Micro Bus 104. The uSBCs execute the same instruction stream in parallel with each other. The Micro Bus 104 is a bidirectional communications bus. The uSBCs support an instruction set with seven basic instruction in it. The instructions are of fixed length and specify either one or two operands only.

Discussion of Applicant's Invention in view of Byers

9. *Byers* discloses a system that includes a microprocessor (μSBC 164 and 166). This microprocessor, by controlling physical layer controllers 130 and 140, processes digital data. ***However, the RISC microprocessor used in the system of Byers is not a "digital signal processor."*** A "digital signal processor" is characterized by an architecture that is optimized

or designed for the processing, usually in real time, of signals which vary over one or more dimensions (*e.g.*, time and/or frequency) and which are represented as a stream of digital samples. These "digital signals" are treated as an ordered sequence of numbers, rather than as text or other general-purpose digital data, and are usually processed arithmetically. Thus, a processor is not a "digital signal processor" unless it is optimized for the efficient arithmetic processing of sequences of numeric digital samples, as opposed to the general processing of digital data.

10. A "digital signal processor" is characterized by one or more of the architectural features discussed below, which are related to: memory access; single-cycle numeric operations; arithmetic overflow or underflow; zero-overhead looping; address generation optimized for arithmetic operations; task-specific hardware acceleration. A particular digital signal processor is not required to include each of these features, but all DSPs incorporate at least one of them.

11. ***Memory Access***: A common operation in many DSP algorithms is a sum of products: $y=\sum xh$. This operation involves: fetching two operands; multiplying the two operands together; accumulating the result. In addition to the memory accesses for the operands and the result, the next instruction must also be fetched. A DSP architecture typically supports multiple memory accesses in the same instruction cycle (*e.g.*, two data accesses and one instruction access) in order to efficiently implement the sum of products. In contrast, processors that are not optimized for DSP algorithms typically use a single bus for both data and instructions, and support a single memory access per instruction cycle.

12. ***Single-Cycle Numeric Operations***: DSP algorithms make heavy use of combined arithmetic operations (*e.g.*, multiply, add, subtract, bit-shift). To complete these multiple operations in a single cycle, a DSP architecture typically provides a specialized unit for each operation. For example, a specialized multiply-accumulate (MAC) unit allows the multiply and add to occur in parallel, and a barrel-shifter can shift samples by more than one bit at a time. Also, each of these specialized units may have its own data path so more than one can be used in the same instruction. In a typical general purpose processor, an instruction can have only one arithmetic or logical operation.

13. ***Arithmetic Overflow or Underflows***: Arithmetic operations in digital signal processing algorithms (*e.g*, multiply-accumulate (MAC) operations) commonly produce overflows and underflows. Digital signal processors often include a feature known as saturation, in which a positive or negative overflow will accumulate at the maximum (or minimum) values that the register can hold. In contrast, a register in a general purpose processor wraps around on overflow, usually from a large positive value to a large negative value or vice versa. Another method of dealing with overflow or underflow in a digital signal processor is to use guard bits. Guard bits extend the storage of the product to more than twice the size of the multiplier input. For example, when multiplying two 16-bit numbers, their 32-bit product is added to a register that is wider than 32 bits, typically a 40-bit register.

14. ***Zero-overhead Looping***: Executing code in a loop is at the core of most DSP algorithms. Therefore, a typical DSP architecture allows loops to execute with no overhead.

In a general purpose processor, loops involve overhead. The executable code increments (or decrements) a counter, and uses a conditional instruction in conjunction with the counter to determine whether execution continues at the top of the loop or outside the loop. In contrast, a DSP architecture uses dedicated hardware to maintain the counter, evaluate the conditional, and determine the address of the next instruction without expending instruction cycles to do so in each iteration of the loop.

15. ***Optimized address generation***: Many digital signal processing algorithms (*e.g.*, digital filters) require data in a range of addresses (a buffer) to be addressed so that the address pointer wraps around from the end of the buffer back to the start of the buffer (buffer length). This pointer movement is called circular buffering. A variation of circular buffering, which is required in some applications, advances the address pointer by values greater than one address per step but still wraps around at a given length. This variation is called modulo circular buffering. Generating the next circular buffer address involves modifying and then comparing the address to determine if a wrap around is needed. The modulo variant requires an extra addition step. A typical digital signal processor has specialized address generation units which perform these operations in hardware for optimum efficiency. In contrast, using a circular buffer with a general-purpose processor requires the wrap around operations to be performed in software, which limits the processor's ability to handle real-time signals. Another specialized form of addressing supported by a typical digital signal processor is bit reversed addressing, used in the Fast Fourier Transform algorithm. This type of addressing reorders a table of values by reversing the order of the address bits. This involves reversing

the order of the bits in each address, and shuffling the data so that the new, bit-reversed, addresses are in ascending order.

16. ***Hardware acceleration***: Many digital signal processors are optimized for a particular function (e.g., transmission and reception of a signal on a certain type of communications channel, according to a defined standard). The DSPs used for such function may be further optimized to include specialized hardware which accelerates specific, highly computationally intensive tasks. An example of such hardware would be a Fast Fourier Transform accelerator within a DSP optimized for Discrete Multitone transmission.

Serial No.: 09/716,787
TKHR Docket No: 061606-1241

DECLARATION

I hereby declare that all statements made herein are of my own knowledge are true and that all statements are made on information and belief and are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Kenneth D. Ko

5.23.05

Date